60/108,648 entitled "Clock Generation and Distribution in an Ethernet Transceiver" filed on November 16, 1998 and Serial Number 60/130,616 entitled "Multi-Pair Gigabit Ethernet Transceiver" filed on April 22, 1999.

A1 Cont.

The present invention is related to the following co-pending applications filed on the same day as the present invention and assigned to the same assignee, the contents of each of which are herein incorporated by reference: Serial Number 09/437,724 entitled "Switching Noise Reduction in a Multi-Clock Domain Transceiver" and Serial Number 09/437,719 entitled "Multi-Pair Gigabit Ethernet Transceiver".

Please insert the following paragraph on page 6, after line 17 and before line 18, as follows:

A2

FIG 5A shows another embodiment for generating the sampling clock signals.

Please amend the second full paragraph on page 15 as follows:

The 4-D output of the trellis decoder 38 is provided to the PCS receive section 204R. The receive section 204R of the PCS block de-scrambles and decodes the symbol stream, then passes the decoded packets and idle stream to the receive section 202R of the GMII block which passes them to the MAC module. The 4-D outputs, which are the error and tentative decision, respectively, are provided to the timing recovery block 222, whose output controls the sampling time of the A/D converter 216. One of the four components of the error and one of the four components of the tentative decision correspond to the receiver shown in FIG. 2, and are provided to the adaptive gain stage 34 of the FFE 26 to adjust the gain of the equalizer signal path. The error component portion of the decoder output signal is also provided, as a control signal, to adaptation circuitry incorporated in each of the adaptive filters 230 and 232. Adaptation circuitry is used for the updating and training process of filter coefficients.

A3

Please amend the paragraph beginning at line 23 on page 24 as follows: